ABSTRACT OF THE INVENTION

A capacitor under bitline DRAM memory cell and method for its fabrication provides a high density memory cell with the capacitor formed in the PMD layer. The memory cell utilizes several variations of storage contact pillar structures as, for example, a storage plate of the memory cell capacitor formed within a trench in the PMD layer. This capacitor plate structure is overlaid with a capacitor dielectric layer which is overlaid with another conductive layer, for example, the M1 layer to form the other capacitor plate. An access transistor formed between substrate active regions and a word line, is in electrical communication with a bit line contact, the storage contact capacitor plate, and the word line respectively. The high density memory cell benefits from the simple standard processes common to logic processes, and in one embodiment requiring only one additional masking step.

S:\TGE\TI\P197US\p197us.pat.doc